REMARKS

In this Response, claim 29 has been canceled without prejudice or disclaimer and claims 13, 44, and 53 have been amended. Support for the amendments can be found in the present application as originally filed. Reconsideration of the outstanding rejection in the present application is respectfully requested based on the following amendment and remarks.

Obviousness Rejection of Claims 13, 15-29, 31-40, 43-50, and 52-54

At page 2 of the Office Action, claims 13, 15-29, 31-40, 43-50, and 52-54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eifrig (US 6,748,020) in view of Pian (US 6,366,614). This rejection is respectfully traversed with amendment.

Independent claim 13 has been amended and presently recites the features of:

a memory;
a memory controller to access the memory;
a first processor to parse received video data to generate a plurality of packets and provide the plurality of packets for storage in the memory, the first processor comprising a general purpose processor;
a second processor comprising a video transcoder; and
a decoder instruction packet (DIP) sequencer to:
access one or more packets of the plurality of packets from the memory via the memory controller;
configure the second processor based on opcodes of the one or more packets; and
provide the one or more packets to the second processor for transcoding.

Eifrig and Pian, individually or in combination, fail to disclose or suggest at least the DIP sequencer feature presently recited by claim 13. To illustrate, neither Eifrig nor Pian discloses or suggests a DIP sequencer that accesses packets from a memory via a memory controller and

provides the packets to a second processor. Nor do Eifrig and Pian disclose or suggest a DIP sequencer that configures the second processor based on opcodes of such packets accessed from memory and provided to the second processor. Accordingly, the proposed combination of Eifrig and Pian fails to disclose or suggest each and every feature of claim 13, as well as the particular combinations of features of those claims depending from claim 13 at least by virtue of this dependency.

Independent claim 44 has been amended and presently recites the features of:

a memory;
a memory controller to access the memory;
a decoder instruction packet (DIP) sequencer to:
access from the memory via the memory controller one or more packets having a video data payload and information related to the video data payload from the memory, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristic represented by a first value; and
configure a first processor based on opcodes of the one or more packets;
the first data processor to transcode the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value; and
a second data processor comprising a general purpose processor, the second data processor to:
receive a data stream including video data at a first data processor;
parse the data stream to identify video data associated with a first channel;
packetize the video data associated with the first channel to generate the one or more packets; and
provide the one or more packets for storage in the memory.

As discussed above with respect to claim 13, neither Eifrig nor Pian discloses or suggests a DIP sequencer that accesses one or more packets having a video data payload from a memory via a memory controller or that configures a first processor based on opcodes of such packets.

Accordingly, Eifrig and Pian, individually or in combination, fail to disclose or suggest at least the DIP sequencer feature presently recited by claim 44. The proposed combination of Eifrig and Pian therefore fails to disclose or suggest each and every feature recited by claim 44, as well as the particular combinations of features recited by claims depending from claim 44 at least by virtue of this dependency.

Independent claim 53 has been amended and presently recites the features of:

packetizing, at the first processor, the video data associated with the first channel to generate the one or more packets, each packet having a video data payload and information related to the video data payload, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristic represented by a first value;

storing the one or more packets at a memory;

accessing the one or more packets from the memory via a decoder instruction packet (DIP) sequencer;

providing, from the DIP sequencer, the one or more packets to a second processor;

configuring, via the DIP sequencer, the second processor based on opcodes of the one or more packets; and

transcoding, at the second processor, the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value.

As similarly discussed above with reference to claims 13 and 44, Eifrig and Pian fail to disclose or suggest accessing one or more packets from a memory via a DIP sequencer and providing the one or more packets to a second processor, much less configuring, via the DIP sequencer, the second processor based on opcodes of the one or more packets as provided by claim 53. The proposed combination of Eifrig and Pian therefore fails to disclose or suggest each and every feature recited by claim 53, as well as the particular combinations of features recited by claims depending from claim 53 at least by virtue of this dependency.

Independent claims 13, 44, and 53 recite subject matter directed to a first processor and a second processor and their respective functionality/operations. For at least the reasons discussed in the Response to Final Office Action mailed March 21, 2008, the proposed combination of Eifrig and Pian fails to disclose or suggest such subject matter.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-1835.

Respectfully submitted,

/Ryan S. Davidson/ May 22, 2008

Ryan S. Davidson, Reg. No. 51,596
LARSON NEWMAN ABEL POLANSKY & WHITE, LLP
5914 West Courtyard Drive, Suite 200
Austin, Texas 78730
(512) 439-7100 (phone)
(512) 439-7199 (fax)

Date